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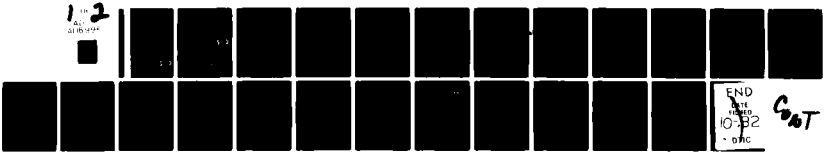

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Systems Technical Memorandum 59

# A FOUR-CHANNEL MULTIPLEXER FOR AN XYZ DISPLAY MONITOR

R.E. SELWAY



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Systems Technical Memorandum 59

# A FOUR-CHANNEL MULTIPLEXER FOR AN XYZ DISPLAY MONITOR

by

R.E. SELWAY



SUMMARY

A four-channel multiplexer was designed and built in early 1974 for the display of low-frequency voltages from an analog computer on a single gun XYZ display monitor. The salient features include the ability to display up to four sets of analog data as either X-Y or Y-T traces on any channel independently of other channels. The equipment has performed satisfactorily in service and is currently also used for the display of analog data generated by digital computer. Improvements in accuracy, speed, component count and reliability could be made with current (1982) technology, but refinements of this nature are not considered necessary.

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CONTENTS

## 1. INTRODUCTION

This memorandum gives a description of the design and construction of a four-channel multiplexer (MUX) for displaying up to four independent sets of analog data on a general purpose XYZ display monitor. The data sets may by X-Y Lissajous figures, or they may be presented as Y-T traces where T is derived from an internal time-base generator. The multiplexer was required for the display of real time, low-frequency data from an analog computer.

It was envisaged that there would not be any demand for great accuracy or stability, only for observing the form of analog data before recording or measuring on other media as necessary. All components were chosen for their ready availability, rather than their quality of performance.

The work was carried out in early 1974 and documented in draft form soon after. Formal publication now, in 1982, is for the purposes of wider dissemination of the information as appropriate.

## 2. CIRCUITS

The overall scheme of the multiplexer is shown in Figure 1. Each X- and Y-input signal is scaled and shifted as required at the first stages of amplification. Then the inputs are multiplexed in pairs, i.e. $X_1$ and $Y_1$, $X_2$ and $Y_2$, etc., to the two second stages which provide the X- and Y-output signals to the monitor.

The time-base generator provides a ramp voltage which may be used instead of the X-input signal for displaying Y-signals against time. The multiplexer logic takes in logic level signals to determine when a particular X-Y corbination is to be displayed. It also provides the pulses required for operating the multiplexer switches in the correct sequence.

### 2.1 Clock

The clock, contained within the box marked 'Multiplexer Logic' in Figure 1, serves to provide the necessary timing pulses to multiplex the analog signals from the computer to the XYZ monitor. The clock frequency was determined by the requirement to display the widest bandwidth data possible without sacrificing dynamic accuracy. The display monitor used with this equipment is a Tektronics model 604 (Ref. 1). The X- and Y-amplifiers of this monitor have a bandwidth to -3 dB of 2 MHz, which effectively limits the bandwidth of an incoming signal to about 200kHz. The clock, generating a square wave, was designed to have frequency of 200 kHz which allowed 2.5 μs for data settling time and 2.5 μs for display time. The clock circuit is taken directly from standard circuits in the manufacturer's data sheets (Ref. 2) and is shown in Figure 2.

## 2.2 Multiplexer Logic and Z-Modulation

The multiplexer logic and Z-modulation circuitry is shown in Figure 3. The clock frequency is divided by two, twice, using two flip-flops (FF) to produce signals which may then be combined in appropriate ways to provide the signals S1 to S4 as depicted in Figure 4.

Formally, let C be the clock state (Figure 4),

then A and B are the outputs from the "÷2" FFs,

then $S1 = \overline{A \wedge B \wedge a}$

$S2 = \overline{\bar{A} \wedge B \wedge b}$

$S3 = \overline{A \wedge \bar{B} \wedge c}$

and $S4 = \overline{\bar{A} \wedge \bar{B} \wedge d}$ ,

where $\wedge$ denotes logical AND,

a denotes channel 1 selected,

b denotes channel 2 selected,

c denotes channel 3 selected,

d denotes channel 4 selected,

and $\bar{}$ denotes the logical inverse.

The clock also provides the timing signal for the Z-modulation of the X-Y signal to the monitor.

If T is the waveform of the time-base blanking signal (see section 2.3) then the Z modulation is given by

$$Z = C \wedge (S1 \vee S2 \vee S3 \vee S4) \wedge T$$

where $\vee$ denotes logical OR.

Details of pin connections on the logic devices shown in all the diagrams may be obtained from the manufacturer's data sheets (Refs. 3 and 4).

## 2.3 Time-base Generator

The maximum sweep frequency of the time-base generator is determined by the requirement not to allow the chopping between channels to be visible on the screen. The chopping period between two adjacent

channels is 5 μs. Since all four channels are multiplexed in sequence the chopping period per channel is 20 μs, i.e. beam ON for 2.5 μs and OFF for 17.5 μs.

The model 604 monitor has a screen graticule measuring 100 mm wide with 10 divisions marked. It was considered that at the highest sweep frequency used each of the four traces should have a minimum of 50 signal samples/division. This means a total of 200 samples/division for all channels. At 20 μs/sample the maximum sweep frequency is therefore equivalent to a minimum sweep time of 4000 μs/division. Using the standard 1,2,5 method of providing sweep time ranges the minimum sweep time selectable was determined as 5 ms/division.

Figure 5 shows the time-base generator circuit. An internally adjustable reference voltage is set up which is integrated in the first amplifier at a rate determined by the RC combination selected. The integrator output is attenuated and buffered at the second amplifier to provide a signal amenable to processing at logic levels in the logic gates following. The first gate acts as a Schmitt trigger, the second combines the triggering inputs (section 2.4) and the third inverts the signal for clocking the monostable multivibrator. The outputs from the monostable multivibrator are used to drive switches Q1 and Q2 to reset the integrator to zero volts output after the Schmitt trigger detects a time-base voltage of +10 V.

## 2.4 External Triggering

Figure 6 shows the circuit used for providing an external trigger pulse. The comparator detects a zero-crossing of the input analog signal. The switch marked + or - serves to gate the comparator output to logic elements which produce a positive pulse on a rising or falling input signal, as appropriate. These pulses are only effective after the 10 V threshold has been reached by the time-base integrator.

The waveforms, with and without external triggering, are shown in Figure 7.

## 2.5 X-Amplifiers

Figure 8 shows the circuit for one channel of X-input. The circuit as far as the summing junction of the last amplifier is duplicated three times to give a total of four separate inputs. The input scaling ranges from 20 V/div to 0.1 V/div. A switch is provided which selects either independent X inputs (for Lissajous-type figures) or the time-base function. A shift control is also provided to position the origin anywhere in the screen. The switches Q1 and Q2 are controlled by the MUX logic signals $S_i$ and $\bar{S}_i$.

### 2.6 Y-Amplifiers

Figure 9 shows essentially the same circuit as for the X-amplifiers with the exception of the time-base input.

### 2.7 Power Supply

The power requirements for the equipment are met by the circuit of Figure 10. The Analog Devices module 920 H supplies ±15 V at 200 mA and the 903 H supplies +5 V at 500 mA.

## 3. CONSTRUCTION

### 3.1 Front Panel

Figure 11 shows the layout of the front panel. The input sockets are arranged as a group of 4 mm banana sockets in the lower right-hand corner. The power on-off switch and indicator lamp are mounted just above. The external trigger input socket is mounted to the left of the indicator lamp and the triggering control switches are situated above the input socket. The sweep time selector switch is mounted in the top right-hand corner.

The X-Y display controls are set up as four columns of six controls which are, from the top, the Y sensitivity, channel selection switch, Y shift, X sensitivity, X or time-base selection switch, and X shift. Miniature components were used where possible in order to reduce the overall size of the equipment, so that the monitor and the multiplexer could fit side-by-side in a standard 19 inch (483 mm) rack.

### 3.2 Printed Circuit Boards

The circuits were laid out on six general purpose printed circuit boards like that shown in Figure 12, one each for ±15 V power supply, X-amplifiers, Y-amplifiers, multiplexer logic and Z-modulation, time-base generator, and +5 V supply. These boards were mounted in a card cage which was fitted into an instrument box measuring 235 mm wide, 148 mm high, and 280 mm deep.

## 4. FURTHER COMMENTS

The equipment was built in early 1974 and hence only reflects the technology readily available at that time. No doubt the circuitry could be modified now (1982) with improvements in accuracy, speed, cost, component count and reliability. However, the equipment has performed to expectations so far and it is not anticipated that any further refinement will be necessary.

## REFERENCES


1. Tektronix CRT Display Systems, Tektronix, Beaverton, Oregon (c.1973).

2. Interface Integrated Circuits, National Semiconductor Corporation, Santa Clara, California, April 1974.

3. Digital Integrated Circuits, National Semiconductor Corporation, Santa Clara, California, June 1973.

4. Linear Integrated Circuits, National Semiconductor Corporation, Santa Clara, California, June 1973.

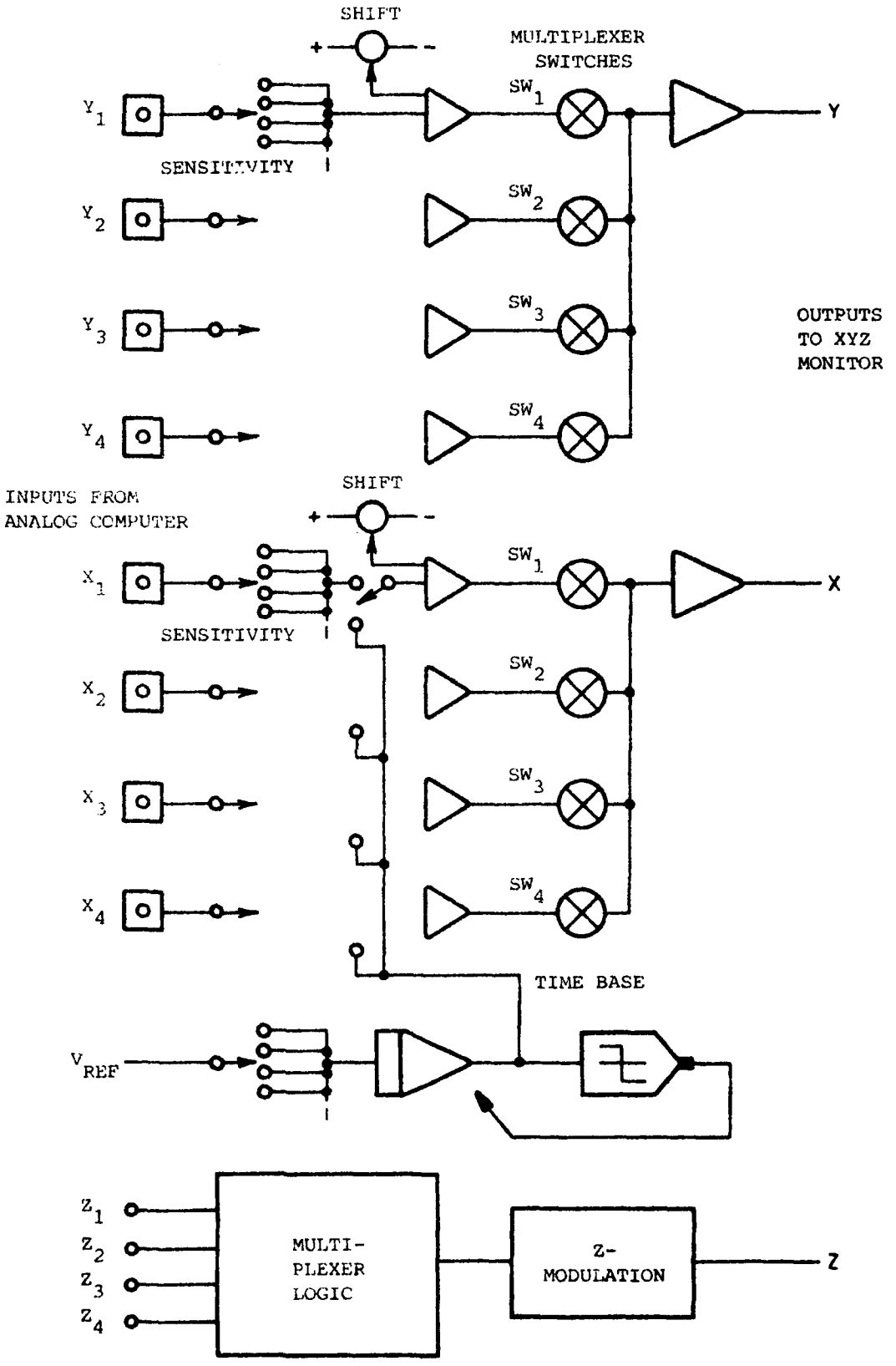
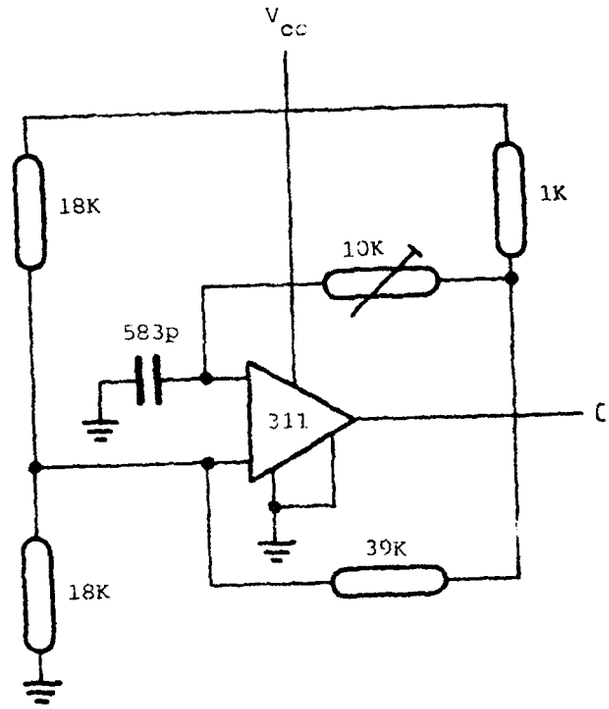



FIG. 1 SCHEMATIC DIAGRAM OF MULTIPLEXER




f = 200 kHz

FIG. 2 CLOCK

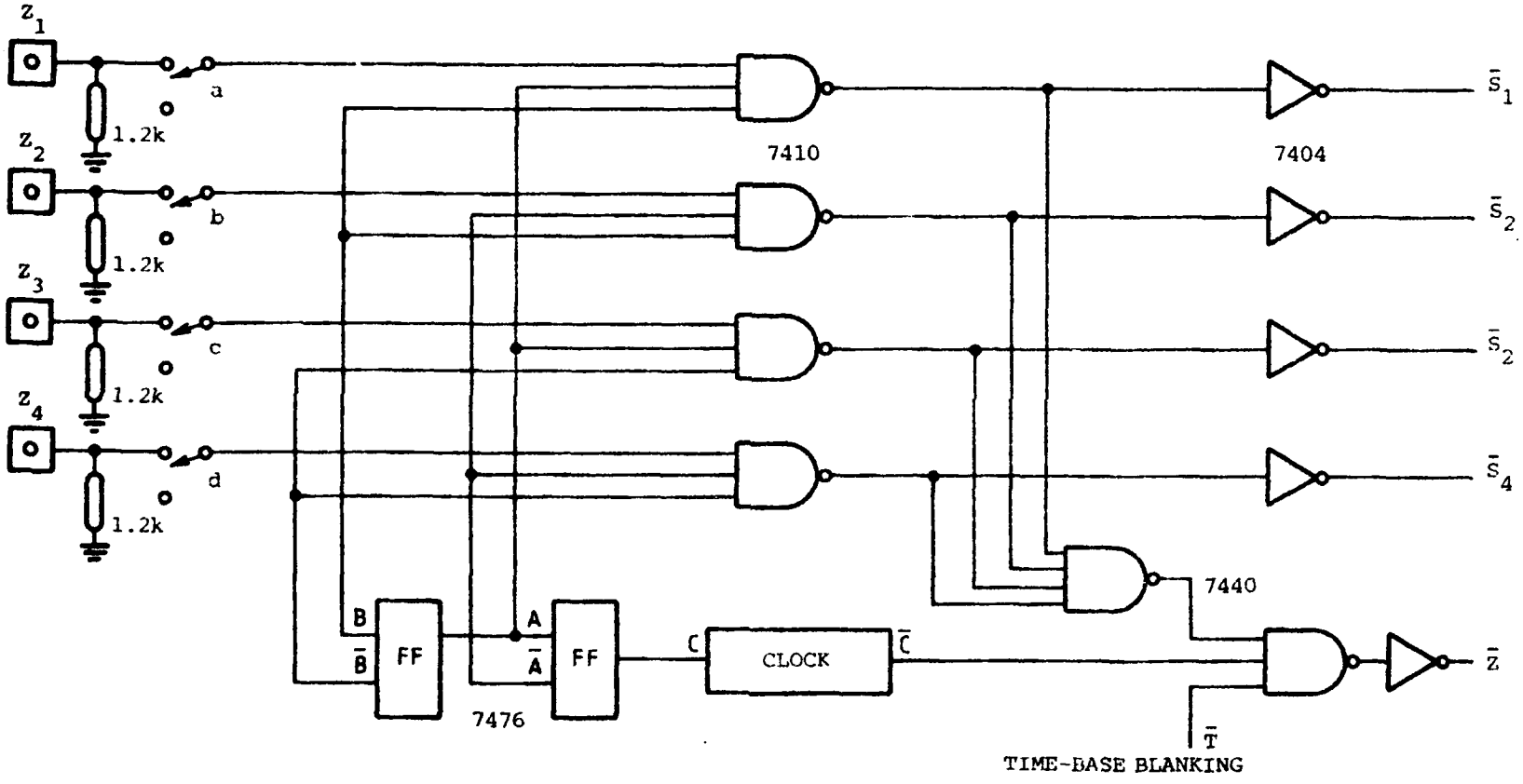



FIG. 3 MULTIPLEXER LOGIC AND Z-MODULATION CIRCUITS

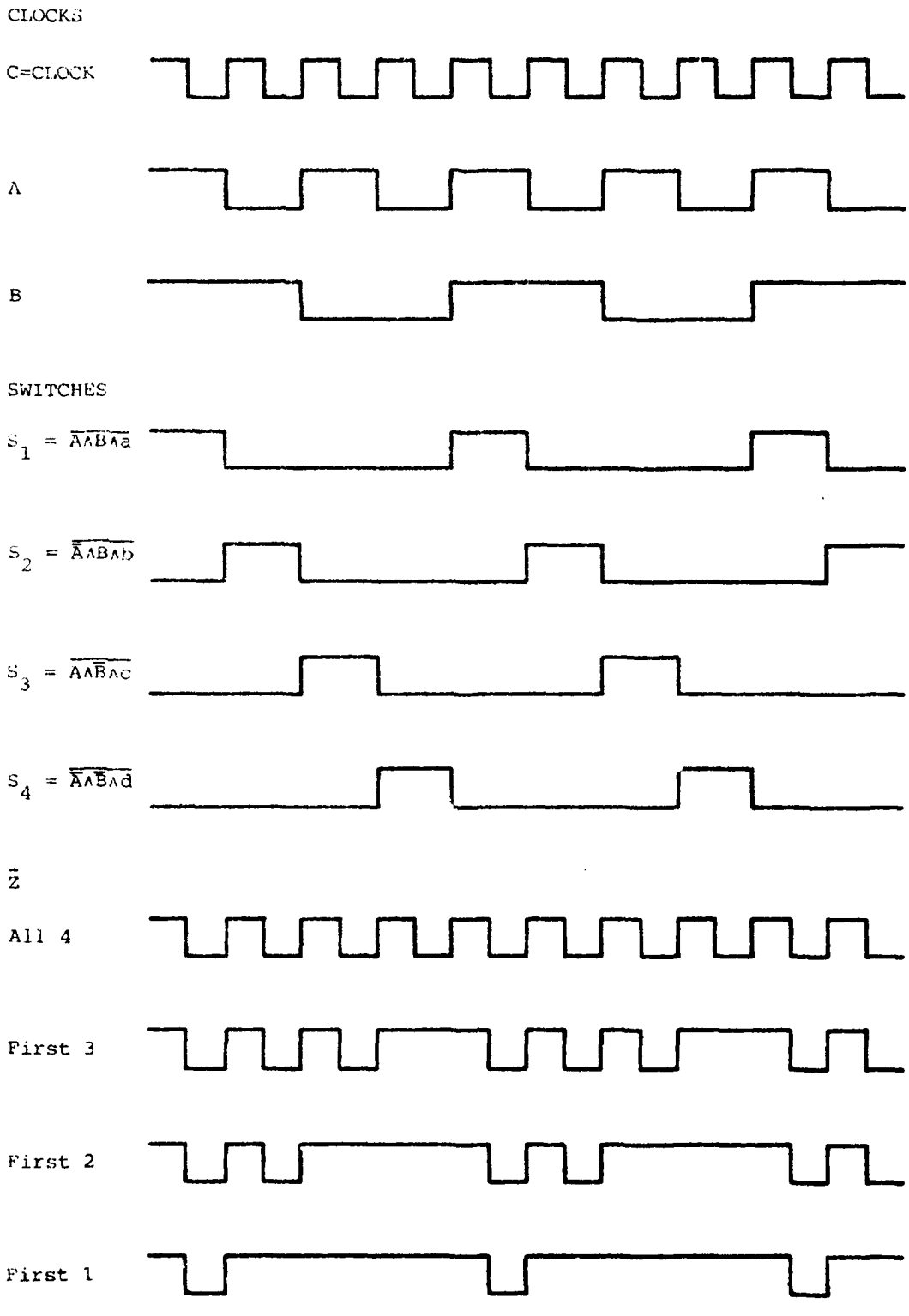



FIG. 4 MULTIPLEXER LOGIC AND Z-MODULATION TIMING

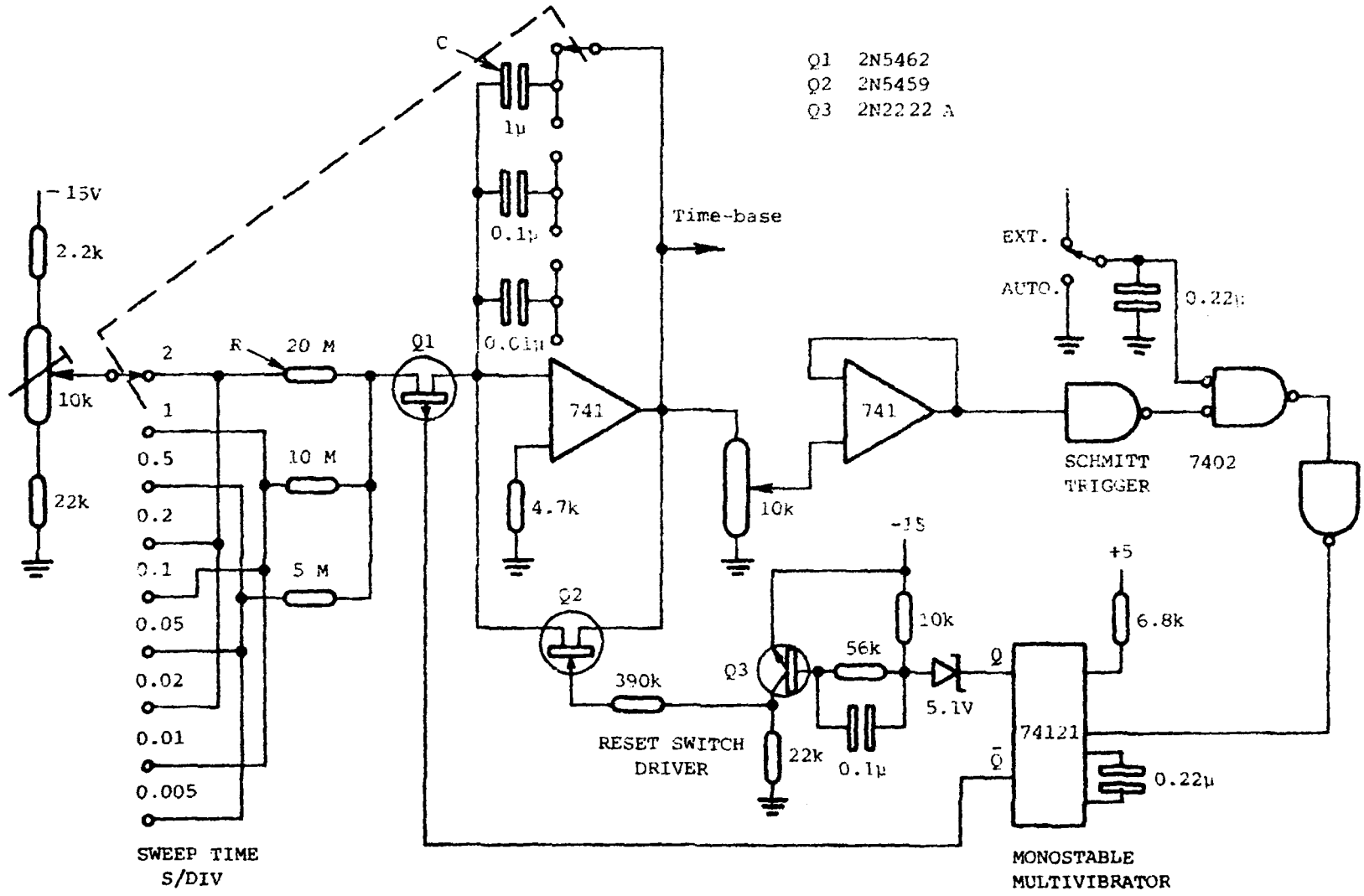
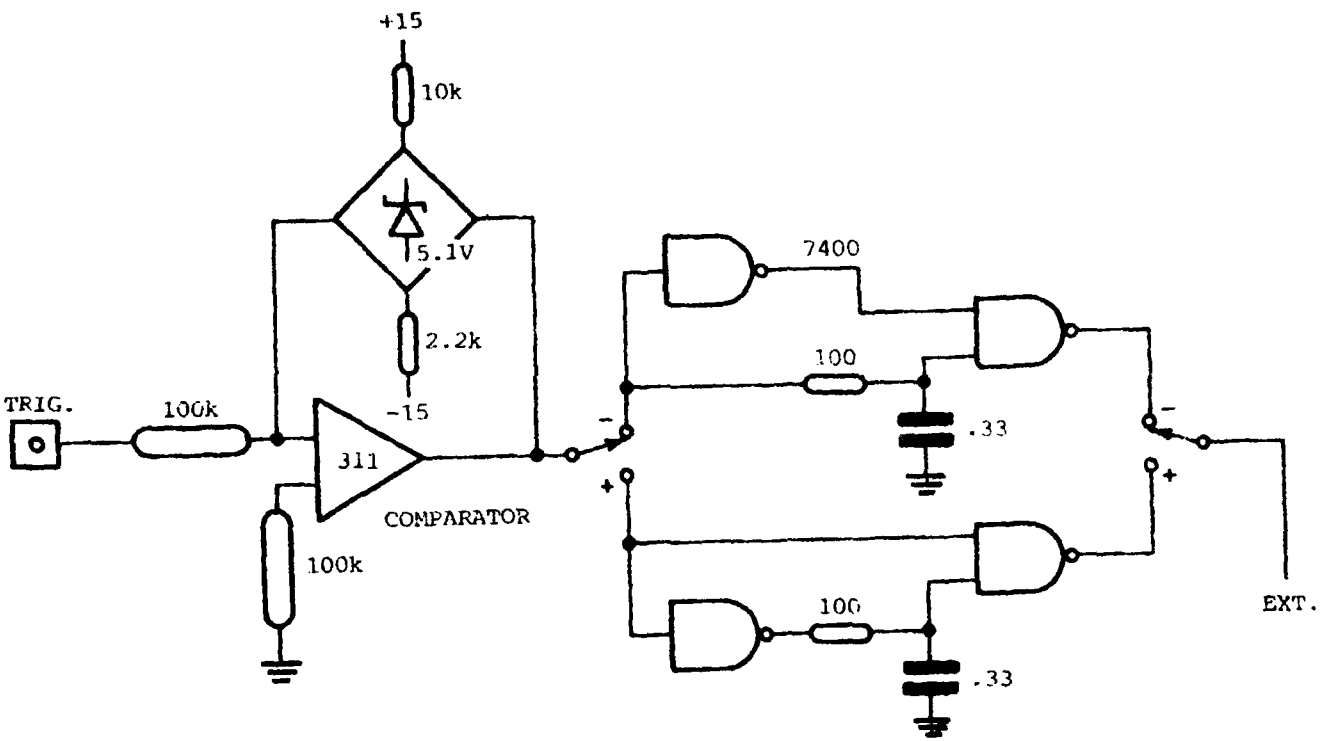



FIG. 5 TIME-BASE GENERATOR




PULSE GENERATOR

FIG. 6 EXTERNAL TRIGGER CIRCUIT

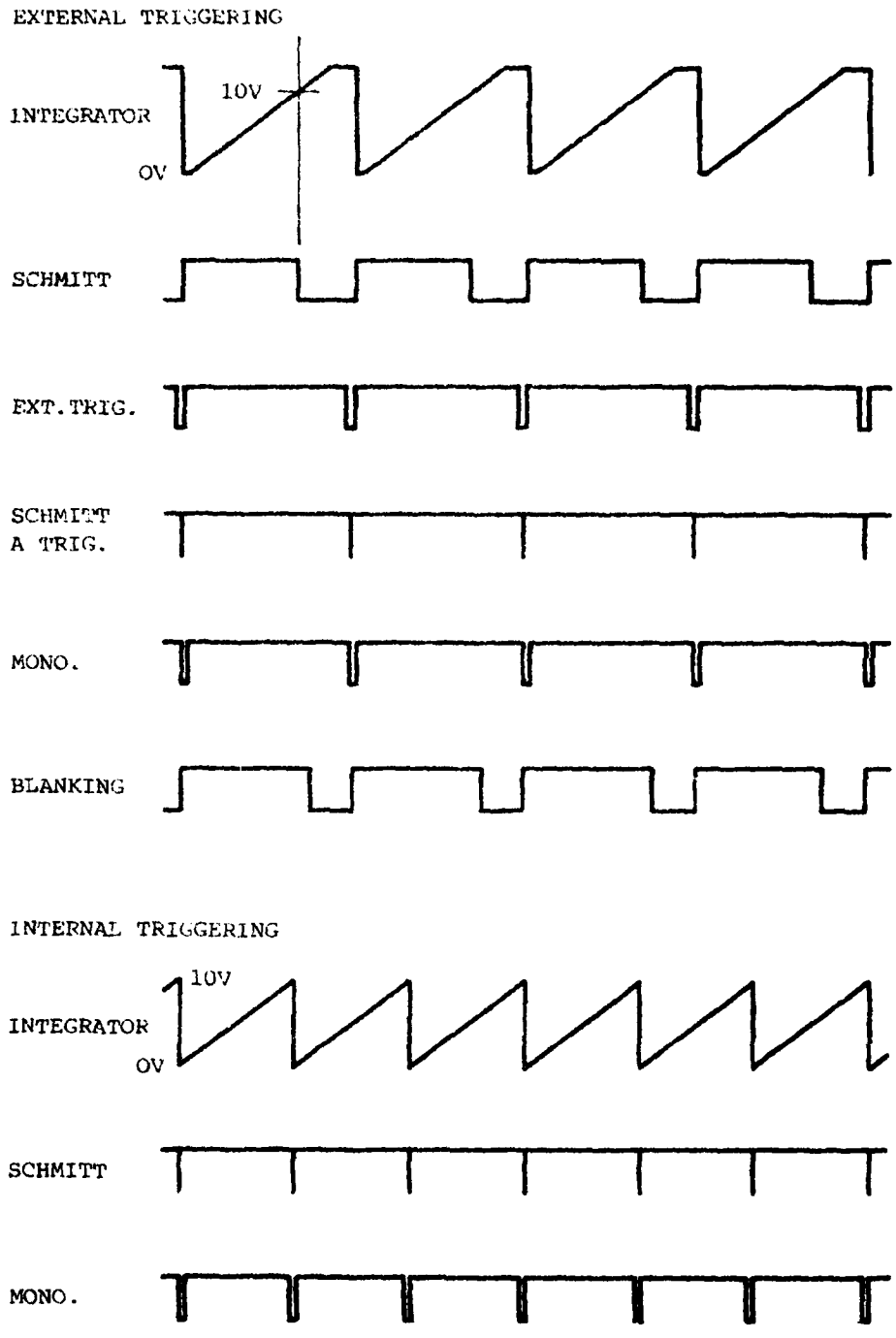
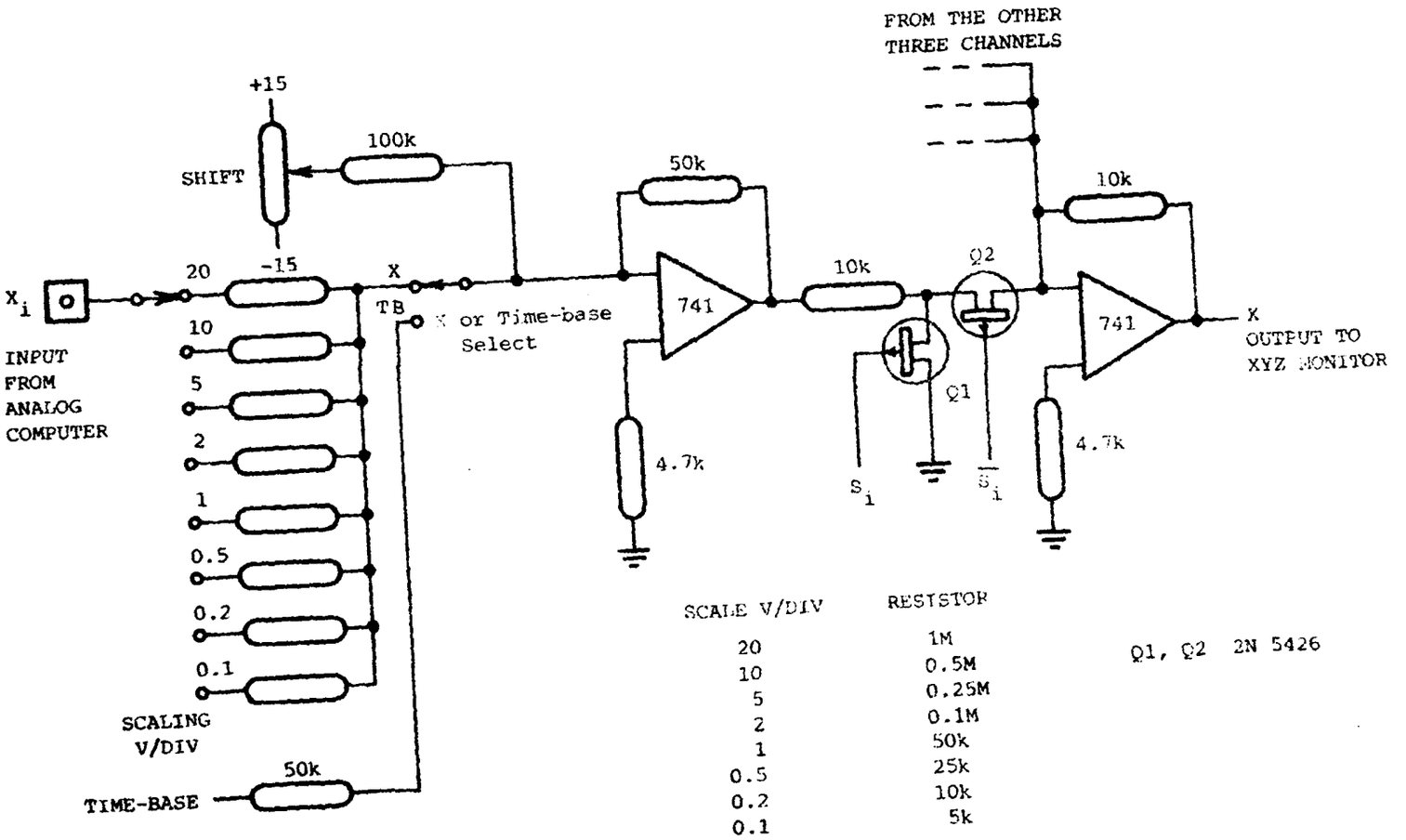


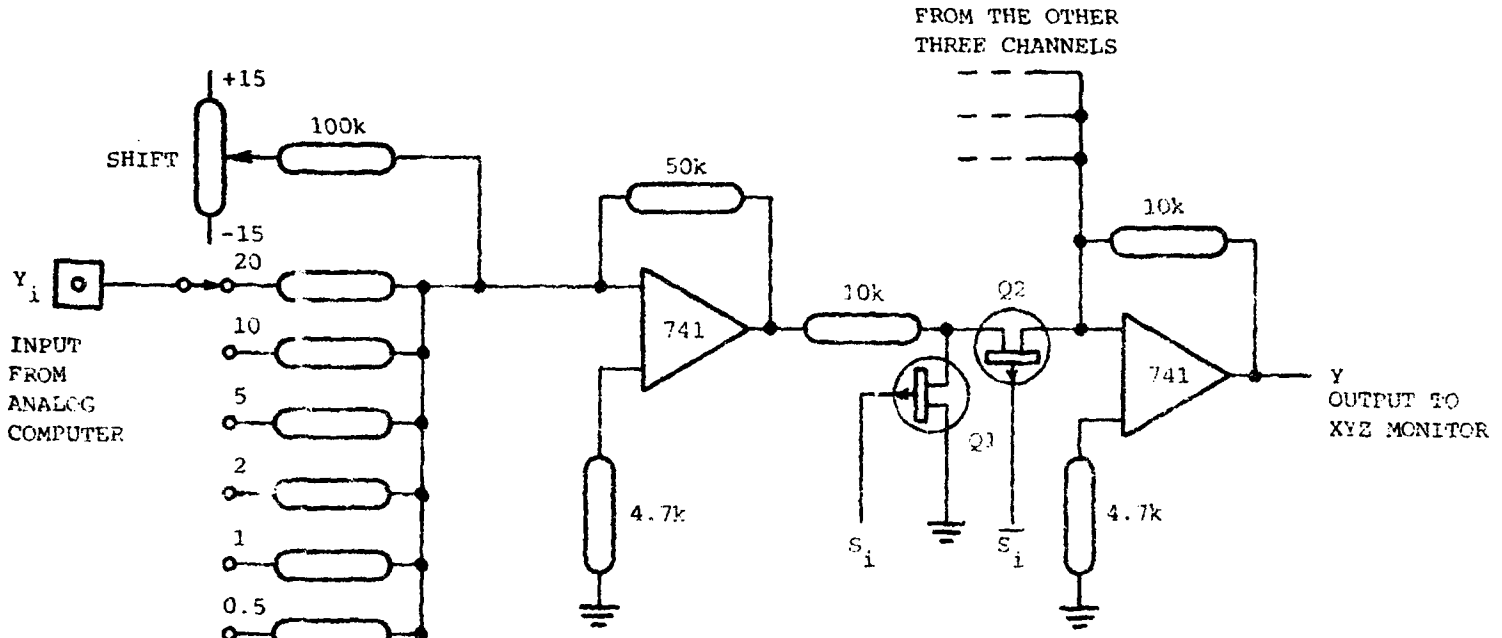

FIG. 7 TIME-BASE WAVEFORMS




| SCALE V/DIV | RESISTOR |
|---|---|
| 20 | 1M |
| 10 | 0.5M |
| 5 | 0.25M |
| 2 | 0.1M |
| 1 | 50k |
| 0.5 | 25k |
| 0.2 | 10k |
| 0.1 | 5k |

Q1, Q2 2N 5426

FIG. 8 X-AMPLIFIER CIRCUIT




| SCALE V/DIV | RESISTOR |
|---|---|
| 20 | 1M |
| 10 | 0.5M |
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| 0.5 | 25k |
| 0.2 | 10k |
| 0.1 | 5k |

Q1, Q2 2N 5426

FIG. 9 Y-AMPLIFIER CIRCUIT

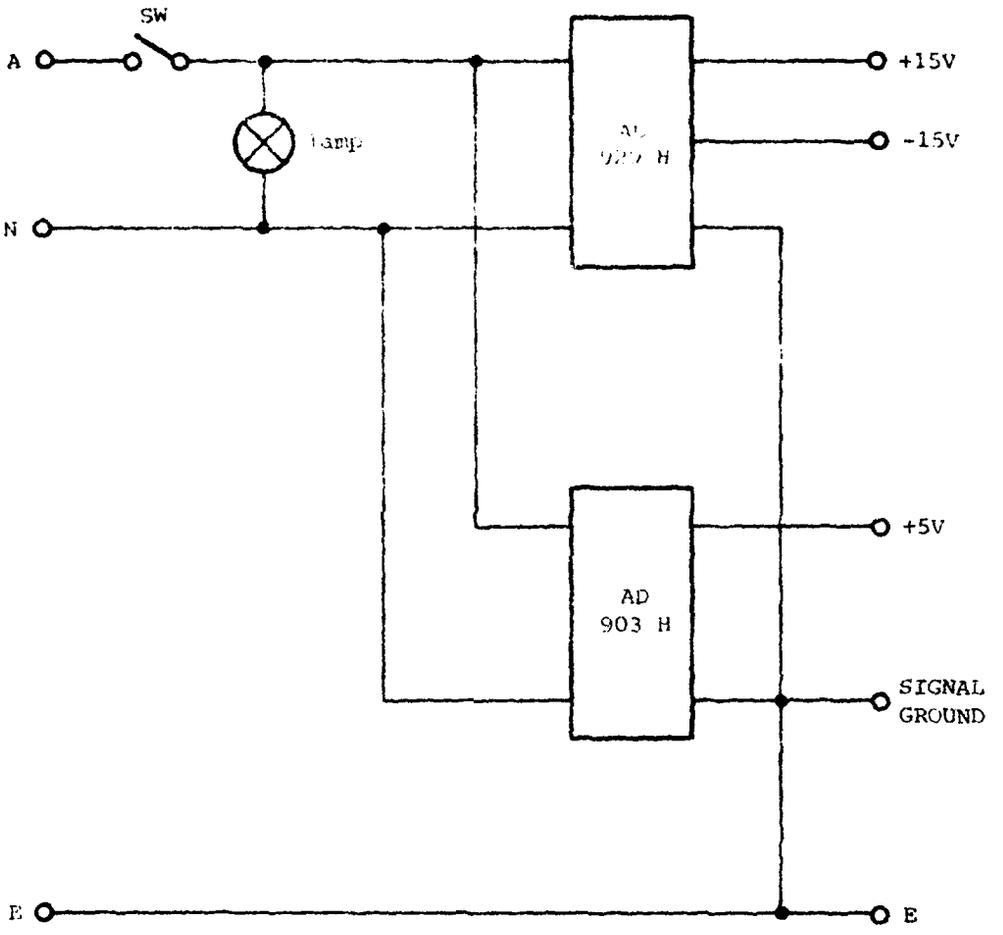


FIG. 10 POWER SUPPLY

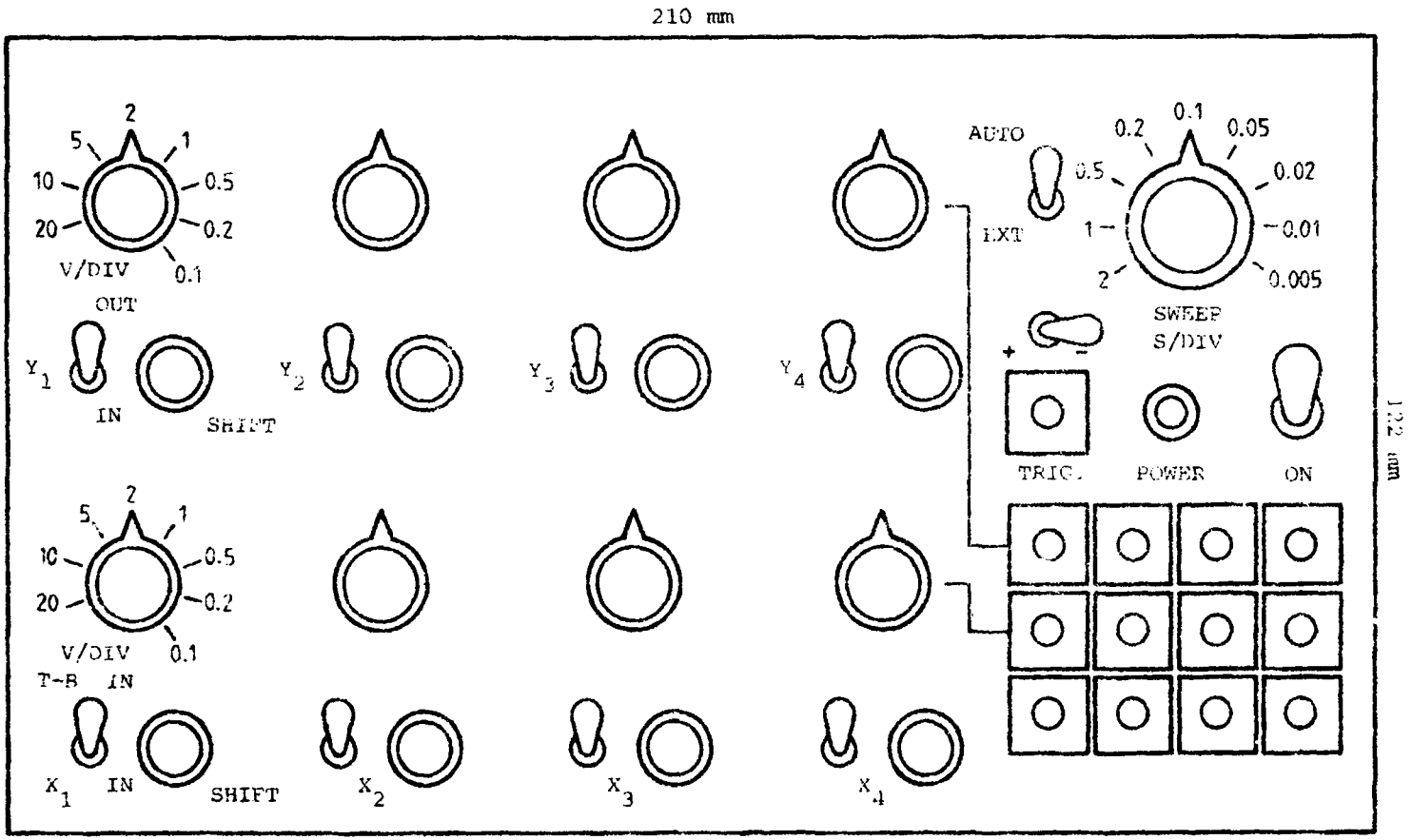


FIG. 11 FRONT PANEL OF MULTIPLEXER

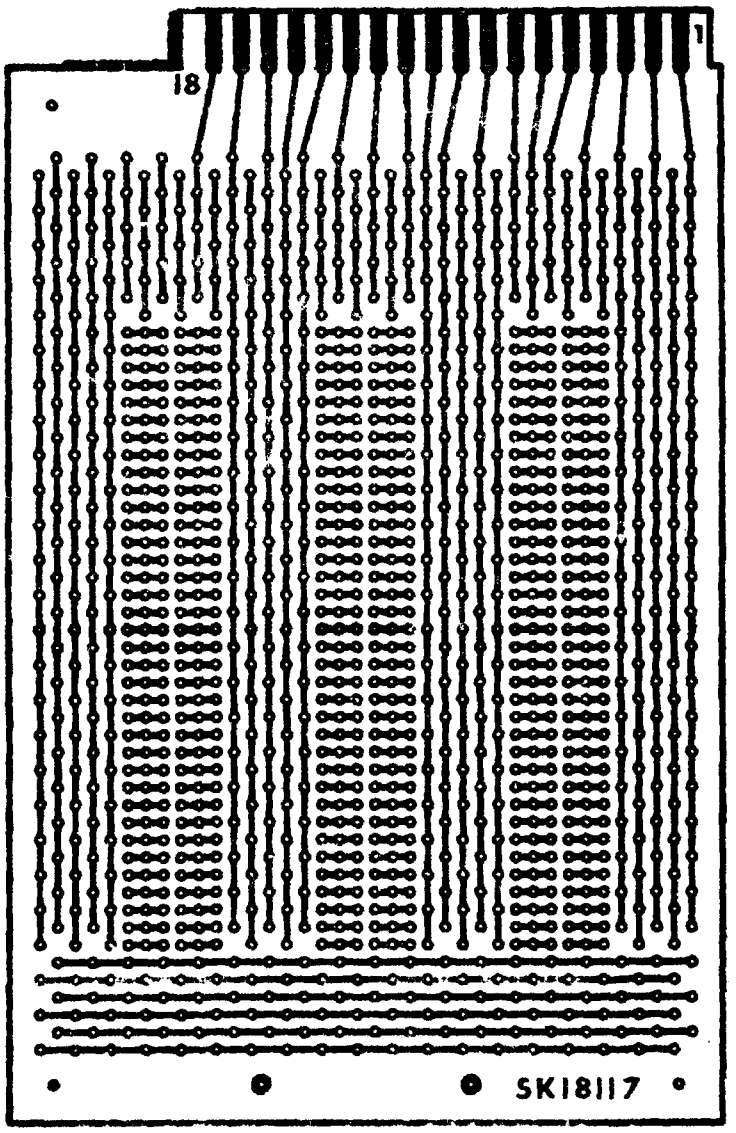


FIG. 12 GENERAL PURPOSE PRINTED CIRCUIT BOARD

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16. Abstract

A four-channel multiplexer was designed and built in early 1974 for the display of low-frequency voltages from an analog computer on a single gun XYZ display monitor. The salient features include the ability to display up to four sets of analog data as either X-Y or Y-T traces on any channel independently of other channels. The equipment has performed satisfactorily in service and is currently also used for the display of analog data generated by digital computer. Improvements in accuracy, speed, component count and reliability could be made with current (1982) technology, but refinements of this nature are not considered necessary.

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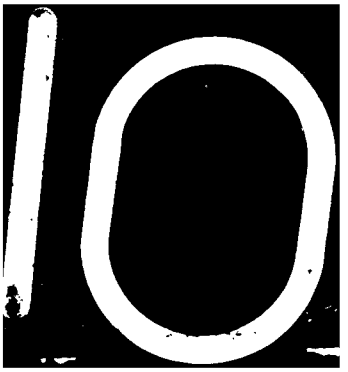

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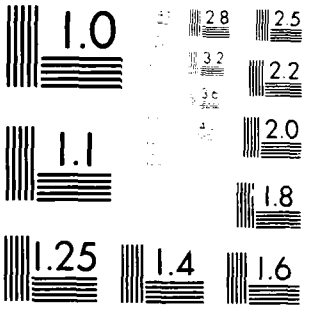

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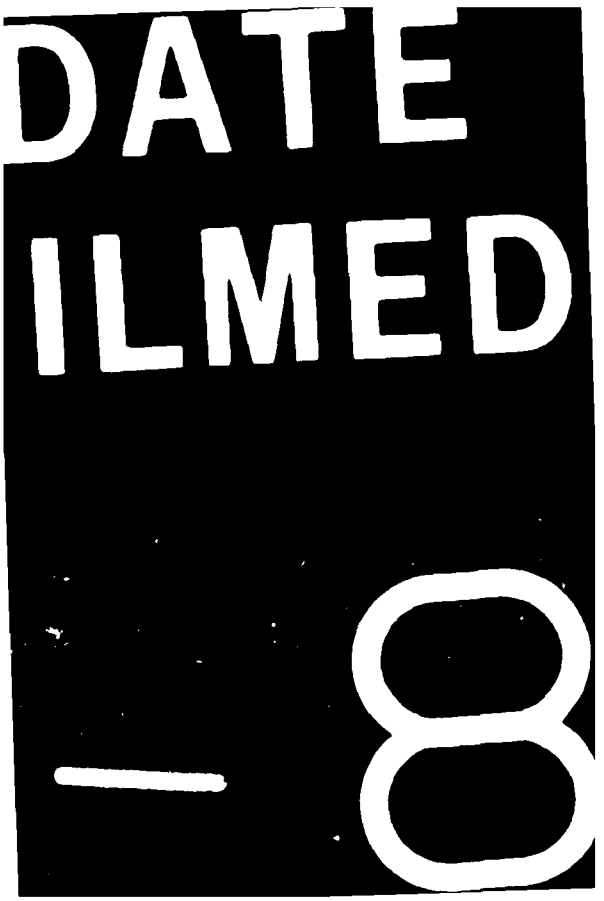
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